

FIG. 1

102221 6828001

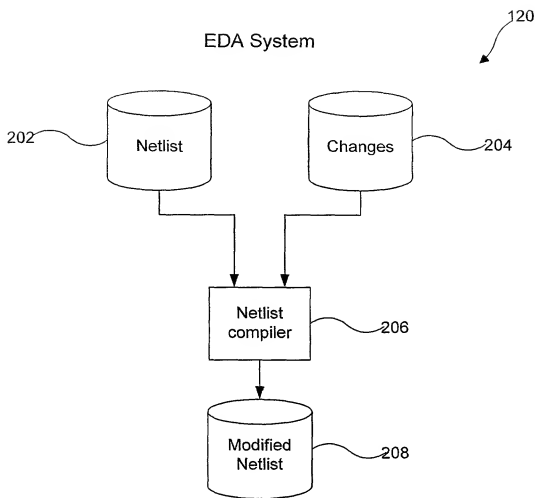


FIG. 2

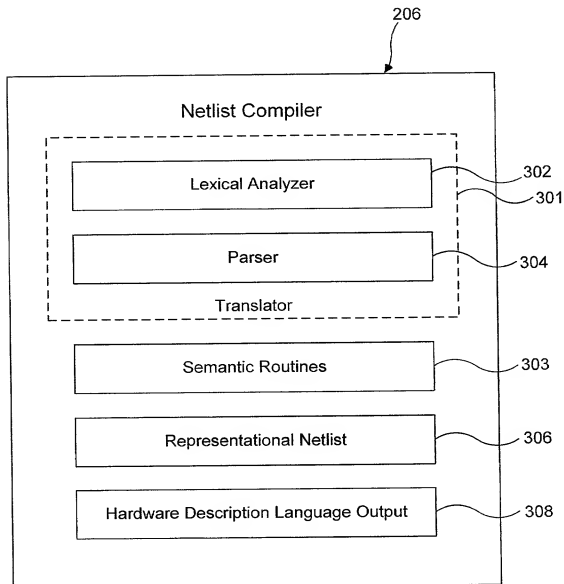


FIG. 3

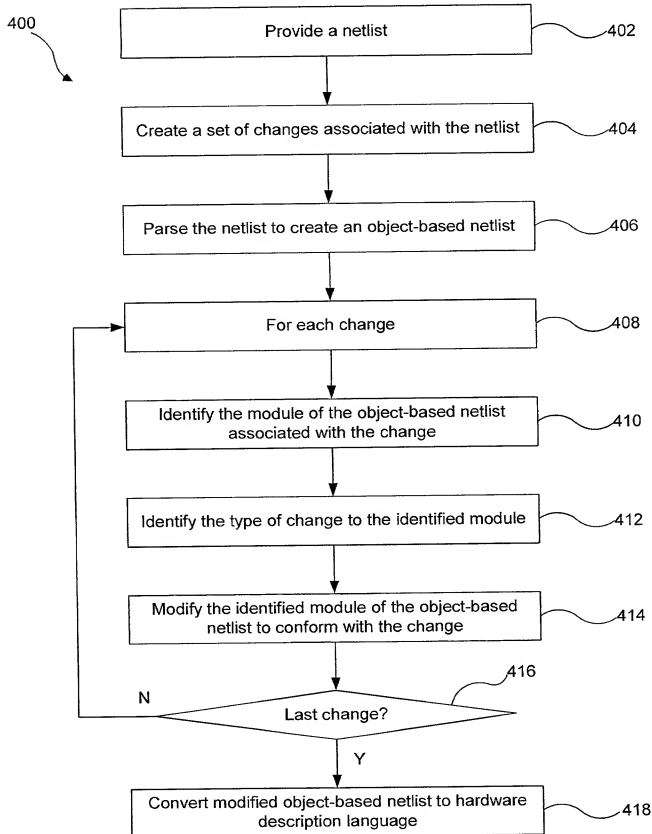


FIG. 4

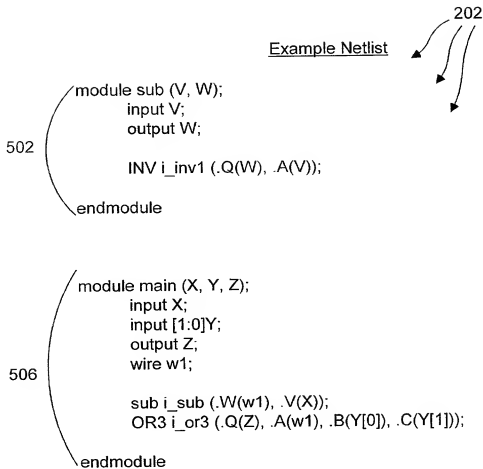
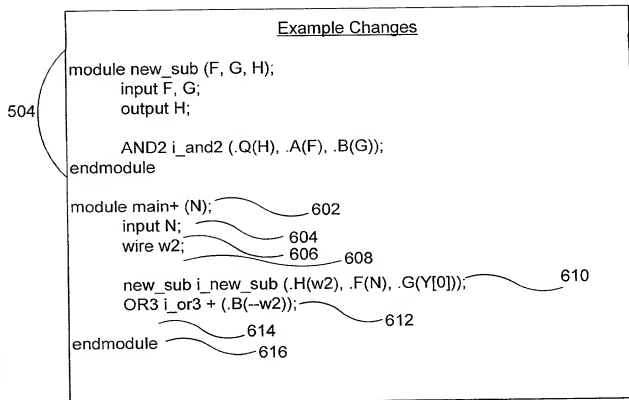


FIG. 5



Example Modified Netlist

```

702 module sub (V, W);
    input V;
    output W;

    INV i_inv1 (.Q(W), .A(V));

endmodule

704 module new_sub (F, G, H);
    input F;
    input G;
    output H;

    AND2 i_and2 (.Q(H), .A(F), .B(G));

endmodule

706 module main (X, Y, Z, N);
    input X;
    input [1:0]Y;
    output Z;
    input N; ← 710
    wire w1;
    wire w2; ← 712

    sub i_sub (.V(X), .W(w1));

    OR3 i_or3 (.Q(Z), .A(w1), .B(w2), .C(Y[1])); ← 714

    new_sub i_new_sub (.F(N), .G(Y[0]), .H(w2)); ← 716

endmodule

```

FIG. 7

208

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